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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,750	03/04/2004	Kenji Takase	0951-0133P	5270

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,750	TAKASE, KENJI	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 10/27/2005 has been reviewed and placed of record in the file.

Claim Rejections - 35 USC § 112

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claim 8** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites: "one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns". It is not clear as to how the one or more dies blank(s) out and shape(s), and to what shape and to what size, the at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns to form the terminal or terminals.

The claimed size(s) and shape(s) of the claimed terminal(s) could not be determined. What are the characteristics of the claimed terminal(s)? Are they round, circular, rectangular, or polygonal? Are they in the microscopic scale? Are the claimed terminals similar to those of the

'782 reference? Are the claimed terminals similar to those of the '857 reference? Are the claimed terminals similar to those of the '327 reference? As has been alleged by Applicant, the terminals of the '782 reference could not have been formed by a die blanking operation (Remark filed 10/27/2005, Page 8), however, no positive evidence has been given); the structure of the '857 reference could not have been formed by a die blanking operation (Remark filed 10/27/2005, Page 9), however, no positive evidence has been given; the terminals of the '327 reference could not have been formed by a die blanking operation (Remark filed 10/27/2005, Page 10), however, no positive evidence has been given. In short, since the claimed size(s) and shape(s) of the claimed terminal(s) could not be determined; the metes and bounds of the claim, as far as "one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns" is concerned, could not be determined, therefore, the claim is indefinite.

With respect to the **argument** that all claimed limitations must be considered, even if they are considered indefinite (Remark filed 10/27/2005, Page 7), it is respectfully pointed out that while it is true that all claimed limitations must be considered, indefinite limitations will not be considered, because they are indefinite, and the indefinite limitation is indefinite because, as detailed above, claimed size(s) and shape(s) of the claimed terminal(s) could not be determined.

With respect to the **argument** that the product-by-process limitation die blanking step should not be considered a non-limitation in the claim, it is respectfully pointed out that the

product-by-process limitation die blanking step should be considered a non-limitation in the instant claim. While it is true that a product-by-process limitation must be considered, it is considered only to a point to determine the patentability of the claimed product, and not the recited steps, as acknowledged by Applicant. And since in the instant case, the claimed size(s) and shape(s) of the claimed terminal(s) resulting from the die blanking step could not be determined – as detailed above - for examination purposes, the limitation "using one or more die to blank out" the at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns to form at least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring has been considered non-limitation. In other words, because the claimed size(s) and shape(s) of the claimed terminal(s) resulting from the product-by-process limitation "using one or more die to blank out" could not be determined, the limitation:

"one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at least as many terminal or terminals of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns" has been interpreted as:

"one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and at least as many terminal or terminals as is or are sufficient for connection to the patterned wiring is or are formed from at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns" for examination purposes.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1 and 8-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Kishita U.S. Patent 5,656,857 (the '857 reference, cited in a previous office action).

The '857 reference discloses in Figures 4-8 and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device in which one semiconductor chip (5; or 20, Fig. 6 or Figs. 7-8) has been mounted onto one substrate (1; or 11) incorporating patterned wiring (generally indicated at 2/3/4, Fig. 6; or generally indicated at 22/18a/32a/33a/13/12...) and the entirety of the one semiconductor chip has been sealed with one resin (7; or 24/25) - meeting the claimed limitation one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins - wherein:

one or more electrically conductive patterns (8, col. 4, lines 56-60; or 12 and/or 33a, columns 1 and 2, particularly column 2, lines 29-30) for shielding is or are formed at one or more end faces at the top of at least one of the substrate or substrates.

With respect to the **argument** that the reference does not disclose one or more electrically conductive patterns be formed at one or more end faces of a substrate (Remark filed 10/27/2005, Page 9), it is respectfully pointed out that the reference does disclose one or more

electrically conductive patterns be formed at one or more end faces of a substrate. See Figs. 6 and 7, reproduced below or next page.

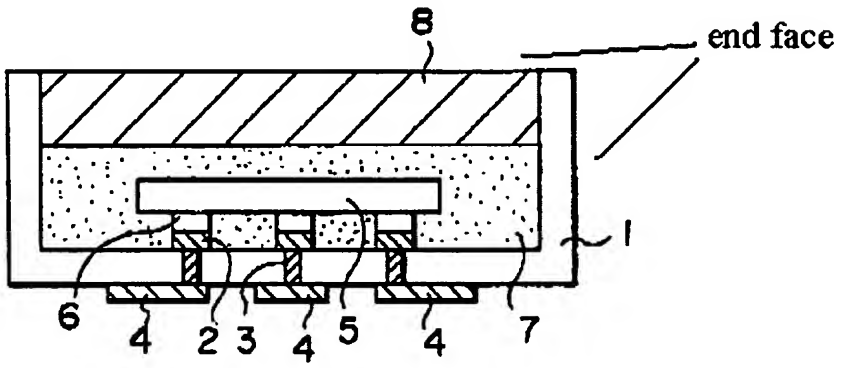


FIG. 6

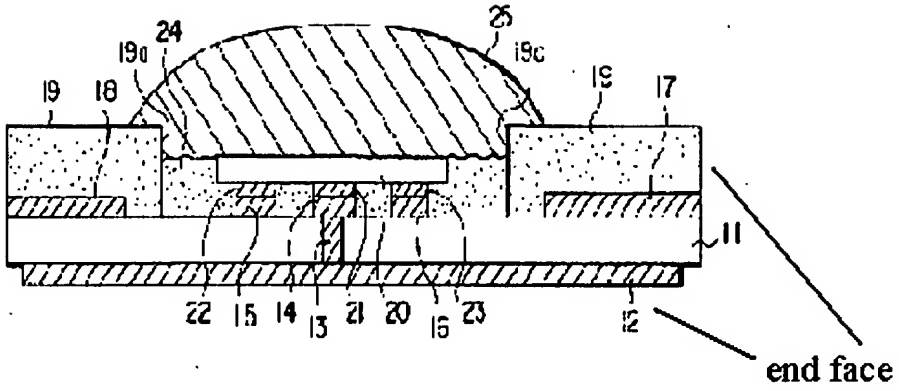
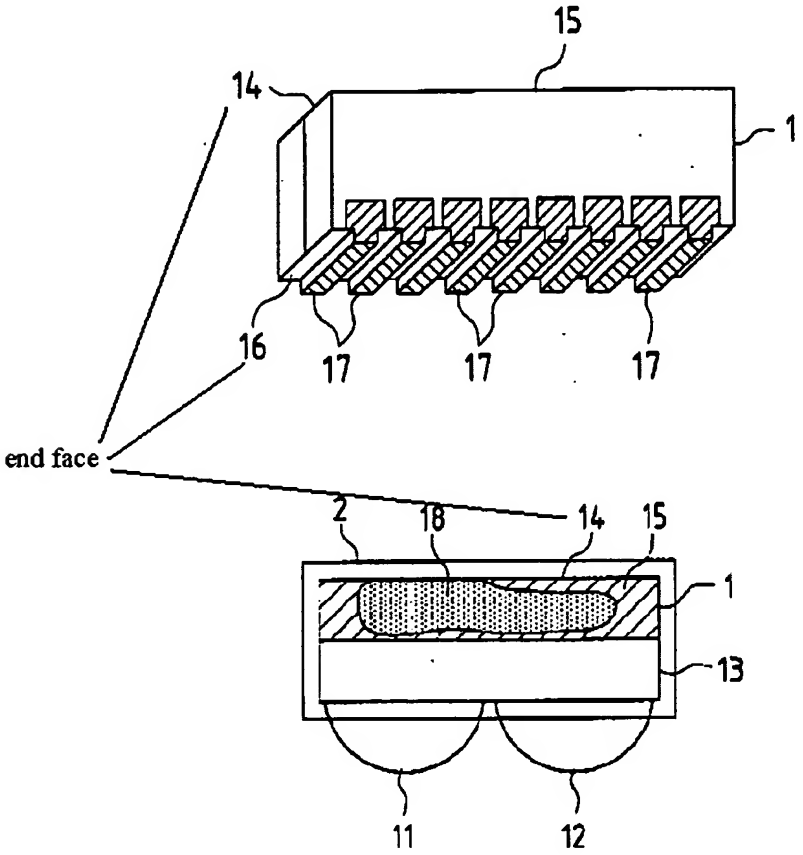


FIG. 7

end face 1. With respect to the **argument** that a top face or a bottom face is not an end face (Remark filed 10/27/2005, Page 9), it is respectfully pointed out that a top face or a bottom face of an element can be considered an end face. The top face or the bottom face of the element defines an end of the element, thus qualifying either the top face or the bottom face of the

element as an end face. The broad interpretation of the term "end face" is reinforced by the fact that Applicant has appeared to indicate such usage. See Figs. 3 and 4 of the present invention, reproduced below or next page, for instances of the usage of "end face". While limitations from the specification shall not be read into the claims during prosecution, claim terminologies are still interpreted in light of the specification.



end face 2. In addition, for the sake of argument, consider the following situation: a device including a semiconductor chip mounted on a "top" face of a substrate, which top face is named T face for identification purposes. The substrate further includes a bottom face, named B face, opposite to the top face, and four "end" faces, named E faces collectively and E1 face, E2

face, E3 face, and E4 face, respectively, all perpendicular to the T face and the B face. In the course of manufacturing the device and in the course of using the device, the device will at times be turned around 90°, a viewer then will perceive the T face and the B face as end faces, and two of the E faces as a top face and a bottom face. Thus it has been shown that every face of the device can be called an end face.

end face 3. In addition, for the sake of clarity, even if a bottom face or a top face could not be considered an end face, the reference still discloses: "...one or more semiconductor chips have been mounted onto a respective mounting face of one or more substrates incorporating patterned wiring... one or more electrically conductive patterns (8, 17 or 12) for shielding is or are formed at one or more end faces at the top (claim 1) or at the bottom (claim 8) of at least one of the substrate or substrates, the one or more end faces being perpendicular to the respective mounting face of one or more substrates", simply because the claimed language does not require that the entirety of the one or more electrically conductive patterns for shielding be formed at one or more end faces at the top or at the bottom of at least one of the substrate or substrates, nor does it require that the one or more electrically conductive patterns for shielding be formed at one or more end faces at the top or at the bottom of at least one of the substrate or substrates so as to substantially cover the one or more end faces.

Referring to **claim 8** and using the same reference characters, citations, interpretations, and responses to arguments as detailed above for claim 1 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and

at least as many terminal or terminals (2, or 3, or 4, or 14, or 18, or 12, or 33a) as is or are sufficient for connection to the patterned wiring (2/3/4; 22/18a/32a/33a/13/12...) is or are formed from at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns.

With respect to the **argument** that the reference does not disclose how the terminals could be formed by blanking as required by the claim (Remark filed 10/27/2005, Page 9), it is respectfully pointed out that, as detailed above in the 112 rejection, since the blanking operation does not result in a non-indefinite terminal with size and shape that could be ascertained so as to establish metes and bounds as required by the respective section of the law, the limitation has been considered non-limitation.

Referring to **claim 9**, the reference further discloses that at least one of the terminal or terminals (4 or 12 or 33a) is formed so as to at least partially protrude to the exterior and so as to have at least one more or less rectangular cross-section (best seen in Fig. 5).

4. **Claims 1-2, 8, and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Juso et al. U.S. Patent Application Publication 20020000327 (the '327 reference, cited in a previous office action).

The '327 reference discloses in the figures, particularly Figures 16's, 1, and 19, and respective portions of the specification a semiconductor device as claimed.

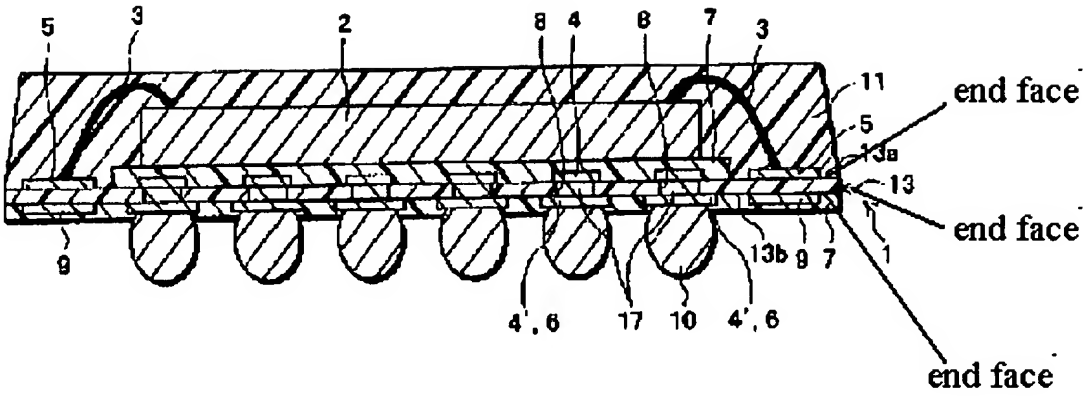
Referring to **claim 1,** the reference discloses a semiconductor device in which one semiconductor chip (2, Fig. 1) has been mounted onto one substrate (generally indicated at 1 and named as wiring substrate by the reference, which wiring substrate 1 comprising at least solder resist 7, insulating substrate 13...) incorporating patterned wiring (generally indicated at 4', 4) and the entirety of the one semiconductor chip has been sealed with one resin (11) - meeting the claimed limitation one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins - wherein:

one or more electrically conductive patterns (4', 4) for shielding (paragraph [0149], and note that, for the record, although the reference only explicitly teaches that copper foil 20 is for shielding, copper foil pattern 4 and 4' also inherently possess shielding property, similar to the present invention) is or are formed at one or more end faces at the top of at least one of the substrate or substrates.

With respect to the **argument** that substrate 1 has nothing on its end faces as required by claim 1 (Remark filed 10/27/2005, Page 9), it is respectfully pointed out that substrate 1 includes one or more electrically conductive patterns (4', 4) on its end faces as required by claim 1.

As detailed above, wiring substrate 1 comprises at least solder resist 7 and insulating substrate 13. The insulating substrate 13, thus the wiring substrate 1 because said wiring substrate 1 comprises said insulating substrate 13, or simply substrate, has a bottom face and a top face that can be considered an end face, and the electrically conductive patterns (4', 4) are formed on its end faces, thus meeting the claimed limitation. See Fig. 1, reproduced below or next page.

FIG.1



For an explanation that a bottom face and a top face can be considered an end face, see paragraphs "end face 1", "end face 2", and "end face 3" above, which include a pictorial comparison with the present invention.

Referring to **claim 8** and using the same reference characters, citations, interpretations, and responses to arguments as detailed above for claim 1 where applicable, the reference discloses a semiconductor device in which one or more semiconductor chips have been mounted onto one or more substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns (4', 4, or 20, Fig. 1 and 16(b)) is or are formed at one or more end faces at the bottom of at least one of the substrate or substrates; and

at least as many terminal or terminals (5) of such number, size, and shape as is or are sufficient for connection to the patterned wiring is or are formed from at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns.

With respect to the **argument** that the reference does not disclose how the terminals could be formed by blanking as required by the claim (Remark filed 10/27/2005, Page 10), it is respectfully pointed out that, as detailed above in the 112 rejection, since the blanking operation does not result in a non-indefinite terminal with size and shape that could be ascertained so as to establish metes and bounds as required by the respective section of the law, the limitation has been considered non-limitation.

Referring to **claim 2**, the reference further discloses that at least one of the electrically conductive pattern or patterns (4', 4) is at least one copper foil pattern (paragraphs [0085] and [0149]).

Referring to **claim 10**, the reference further discloses that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (paragraph [0084]).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 3-4** are rejected under 35 U.S.C. §103(a) as being unpatentable over Juso et al. U.S. Patent Application Publication 20020000327 (the '327 reference) as applied to claims 2 and 18 above, and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492 (cited in a previous office action).

The '327 reference discloses a semiconductor device substantially as claimed and as detailed above including the copper foil or the least one of the copper foil pattern or patterns, but fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the '327 reference such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the coper foil.

6. **Claims 1-3, 5, 7-10 and 13-15** are rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art (APA, Figs 7-9) in view of Inoue et al. U.S. Patent 5,270,493.

APA discloses a semiconductor device substantially as claimed including IC chips that are susceptible to magnetic noise (present invention, paragraph [0007]) and formed on a substrate carrier, but fails to teach an adequate shielding as claimed. Specifically, the APA fails to disclose a copper foil or copper foil pattern or patterns at an end face of the substrate carrier as claimed.

Inoue, in disclosing a substrate carrier (a printed circuit board) for semiconductor devices, teaches that a copper foil or copper foil pattern or patterns at an end face of the substrate carrier provides excellent electromagnetic shield effect (columns 4 and 12, particularly column 4, first paragraph and column 12, last paragraph).

Therefore, it would have been obvious to form the APA's device such that it includes a copper foil or copper foil pattern or patterns at an end face of the substrate carrier. One would have been motivated to make such a change in view of the teachings in Inoue that such a change provides excellent electromagnetic shield effect.

Referring to **claim 10**, Inoue further teaches that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (column 6, lines 15-23)

With respect to the **argument** that Inoue does not disclose shielding patterns on the "ends" of a substrate under normal meaning of the world "end" (Remark filed 10/27/2005, Page 10), it is respectfully pointed out that Inoue does disclose shielding patterns on the "ends" of a substrate under normal meaning of the world "end". For an explanation that a bottom face and a top face can be considered an end face, see paragraphs "end face 1", "end face 2", and "end face 3" above, which include a pictorial comparison with the present invention.

7. **Claims 4 and 6** are rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art (APA, Figs 7-9) in view of Inoue et al. U.S. Patent 5,270,493 as applied above for claims 1-3, 5, 7-10 and 13-15, and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492.

The APA device modified in view of Inoue is a semiconductor device including the copper foil or the least one of the copper foil pattern or patterns, but fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the APA device modified in view of Inoue such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the coper foil.

8. **Claims 1-3, 5, 7-10 and 13-19** are rejected under 35 U.S.C. §103(a) as being unpatentable over Horio et al. U.S. Patent 6,590,152 (the '152 reference) in view of Inoue et al. U.S. Patent 5,270,493.

Similarly to APA, the '152 reference discloses a semiconductor device substantially as claimed including IC chips (2A, 2B, 2C, Fig.4) that are susceptible to magnetic noise (the '152 reference, column 1, lines 15-20) and formed on a substrate carrier (10) including conductive pattern (12) and terminals (12b, Fig. 5), but fails to teach an adequate shielding as claimed. Specifically, the '152 reference does not disclose a copper foil or copper foil pattern or patterns at an end face of the substrate carrier as claimed.

Inoue, in disclosing a substrate carrier (a printed circuit board) for semiconductor devices, teaches that a copper foil or copper foil pattern or patterns at an end face of the substrate carrier provides excellent electromagnetic shield effect (columns 4 and 12, particularly column 4, first paragraph and column 12, last paragraph).

Therefore, it would have been obvious to form the '152 reference's device such that it includes a copper foil or copper foil pattern or patterns at an end face of the substrate carrier. One would have been motivated to make such a change in view of the teachings in Inoue that such a change provides excellent electromagnetic shield effect.

With respect to the **argument** that Inoue shows ends of a substrate that are uncovered (Remark filed 10/27/2005, Page 11), it is respectfully pointed out that Inoue does show ends, such as a top end and a bottom end, of a substrate that are covered. For an explanation that a bottom end face and a top end face can be considered an end face, see paragraphs "end face 1", "end face 2", and "end face 3" above, which include a pictorial comparison with the present invention.

With respect to the **argument** that the references do not disclose terminals having the structure required by claim 8 (Remark filed 10/27/2005, Page 11), it is respectfully pointed out that, as detailed above in the 112 rejection, since the blanking operation does not result in a non-indefinite terminal with size and shape that could be ascertained or structure characteristics that are tangible and measurable so as to establish metes and bounds as required by the respective section of the law, the limitation has been considered non-limitation.

Referring to **claim 10**, Inoue further teaches that at least one gold plating is applied to at least one end face of at least one of the terminal or terminals (column 6, lines 15-23)

Referring to **claims 7 and 15**, because the '152 reference discloses that a silver is not necessary (column 8, lines 10-20), a silver paste could be used.

9. **Claims 4 and 6** are rejected under 35 U.S.C. §103(a) as being unpatentable over Horio et al. U.S. Patent 6,590,152 (the '152 reference) in view of Inoue et al. U.S. Patent 5,270,493 as applied above for claims 1-3, 5, 7-10 and 13-19 and further in view of knowledge in the art as disclosed by McKaveney U.S. Patent 4,447,492.

The '152 reference's device modified in view of Inoue is a semiconductor device including the copper foil or the least one of the copper foil pattern or patterns, but fails to teach that a gold plating is applied over the copper foil or at least the least one of the copper foil pattern or patterns.

However, as is known, copper is prone to oxidation which increases resistance, and it has been customary to plate copper with gold, to prevent oxidation of copper (see, for example, McKaveney, column 1, lines 45-64).

Therefore, it would have been obvious to form the copper foil or the least one of the copper foil pattern or patterns of the '152 reference's device modified in view of Inoue such that the copper foil or the least one of the copper foil pattern or patterns include(s) a gold plating. One would have been motivated to make such a change in view of knowledge in the art, as disclosed by McKaveney, as an example, that such a plating of gold prevents oxidation of the coper foil.

Conclusion

10. Applicant's arguments with respect to the claims, filed 10/27/2005, have been fully considered but they are not persuasive, as detailed above.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
December 29, 2005